

10/031672

FILED UNDER 35 U.S.C. 371

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

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APPL NUM 10031672	FILING DATE 09/09/2002	CLASS 326	SUBCLASS 10	GAU 2819	EXAMINER J. Cho
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****APPLICANTS:** Athas William; Tzartzanis Nestor; Mao Weihua; Peterson Lena;

OK-gc

****CONTINUING DATA VERIFIED:**
This application is a 371 of PCT/US00/19608 07/18/2000
which claims benefit of 60/144,520 07/19/1999
and claims benefit of 60/174,509 01/05/2000

OK-gc

**** FOREIGN APPLICATIONS VERIFIED:**
DONE-gc

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 119 conditions met	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	18036-24199
Verified and Acknowledged Examiners's initials <i>gc</i>		
TITLE : High-performance clock-powered logic		

U S DEPT. OF COMM./PAT. & TM. PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Assistant Examiner	Total Claims
			Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drawg.	Figs. Drawg.
			Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner	Application Examiner
		PREPARED FOR ISSUE	
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